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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,165	01/18/2002	Katsuhiko Fukasaku	NE253-US	7604

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EXAMINER
IM, JUNGHWA M

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,165	FUKASAKU, KATSUHIKO	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *4-6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 7-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 17, 18, 20 and 21 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1 recites one of the source and drain is thinner than the other. There is no disclosure of a thinner source/drain region in the original disclosure. What is a thinner source/drain region any way?

Regarding claims 17, 18, 20 and 21, it is not clear from the original specification how a source/drain region can comprise impurity at an energy level. It appears that impurity at an energy is new matter.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 7-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamane et al. (US 6,020,229), hereafter Yamane in view of Mori et al. (US 6,376,879).

Regarding claims 1-3, Fig.10 of Yamane shows a semiconductor device comprising:

a plurality of transistors on formed on a substrate 201 comprising 1/O-purpose MOSFET (col. 8, lines 38-40) with a thicker gate insulator film (30nm) and a thicker gate electrode (200nm) than a core-purpose MOSFET (LV transistor; col.9, line 5) which has a thickness of 10nm for a gate insulator film and 100nm for a gate electrode; and the said gate electrode includes an impurity to suppress depletion when forming a source region and a drain region (col.8, lines 42-44).

Yamane does not show a device with Ldd formation. However, Fig. 9 of Mori shows a device with Ldd formation in HV transistor and Normal transistor which have different sizes in a gate insulator film and a gate electrode. It would have been obvious to one of ordinary skill to combine the teaching of Mori and Yamane in order to have Ldd regions since a Ldd structure performs functions of increasing the breakdown voltage , migrating of the hot carriers and inhibiting short channel effect as recited in col. 2, lines 48-51.

Regarding claims 7-10, Fig.8 of Mori shows a first Ldd region in a high voltage transistor and a second Ldd region in a normal transistor. And the Ldd region 26b of the high voltage transistor is deeper than the Ldd region 26a of a normal transistor. Note that higher voltage transistor is larger than a normal transistor of a lower voltage (col. 8, lines 58-59 and col. 5, lines 23-31) In addition, Yamane discloses that a cell region is a low voltage element (col. 1, lines 59) and a thick gate oxide region for high voltage element (col.1, lines 23-31). Therefore, it would have been to one of ordinary skill in the art to form deeper drain region including LDD

regions as suggested by Mori to withstand higher operating voltage.

Claims 11 and 12 are identical to claim 3 and Yamane and Mori apply to claim 11 and 12.

Regarding claims 13 and 14, Mori discloses an operational voltage for a high voltage transistor (col. 3, lines 33-36) and a low voltage transistor (col. 4, lines 8-11). It would have been obvious to one of ordinary skill in the art at the time of the invention made to select specific supply voltage as claimed based on operational and integration requirements of the integrated circuit.

Regarding claims 15 and 17, Mori discloses a P-well formation for a HV and a LV transistors (21; col. 11, line 25 and col. 12, line 21) and a N type impurity formation using phosphorous and arsenic(col. 15, lines 24-45).

Regarding claims 16 and 18, Mori discloses a density for phosphorous and arsenic (col. 15, lines 24-45). In addition it would have been obvious to one of ordinary skill in the art at the time of the invention made to have an intended value for a density for phosphorous and arsenic in a HV and a LV regions as claimed, since it has been that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claims 19, Fig.8 of Mori discloses said plurality of transistors comprise a plurality of sidewalls, said plurality of sidewalls comprising a first sidewall 25b and a second sidewall 25a, and wherein said first sidewall has a height greater than that of said second sidewall.

Regarding claims 20, Mori discloses said plurality of transistors comprise said source

region and said drain region with an N - type impurity at a predetermined density and a predetermined energy level and said N - type impurity comprises arsenic (col. 16, lines 53-59).

Regarding claim 21, Mori discloses a density for arsenic (col. 16, lines 53-59)

In addition it would have been obvious to one of ordinary skill in the art at the time of the invention made to have an intended value for a density for arsenic diffusion in a source and a drain recited in pending claim, since it would have been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Also see col. 6, lines 57-61 of the specification of Yamane.

Regarding claim 22, Yamane discloses a semiconductor device comprising: a plurality of transistors having different gate insulator film thickness values, said plurality of types of transistors having different thickness values of a gate electrode thereof in correspondence to the thickness values of the gate insulator film as discussed in claim 1.

Yamane does not show a device with Ldd formation. However, Fig. 9 of Mori shows a device with Ldd formation in HV transistor and Normal transistor which have different sizes in a gate insulator film and a gate electrode. It would have been obvious to one of ordinary skill to combine the teaching of Mori and Yamane in order to have Ldd regions since a Ldd structure performs functions of increasing the breakdown voltage , migrating of the hot carriers and inhibiting short channel effect as recited in col. 2, lines 48-51.

Regarding claim 23, Yamane discloses a semiconductor device comprising: a plurality of transistors having different gate insulator film thickness values with a polysilicon film layer, said

plurality of transistors having different thickness values of a gate electrode thereof in correspondence to the thickness values of the gate insulator film as discussed in claim1. Even though Yamane does not explicitly teach the thickness of said gate insulator film varies based on the amount of deposited gate electrode materials, it is obvious that the gate insulator thickness has to be adjusted according the amount of deposited gate electrode materials which determines the thickness of the gate electrode in order to have a proper noise suppression from the substrate.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (703) 305-3998. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmi
March 10, 2003

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800